A–1137

Total Pages : 4 **Roll No. .....**

BCA(N)-120

Digital Electronics

Examination, June 2025

Time : 2:00 Hrs. Max. Marks : 70

Note* :–** This paper is of Seventy (70) marks divided into Two (02) Sections 'A' and 'B'. Attempt the questions contained in these Sections according to the detailed instructions given therein. ***Candidates should limit their answers to the questions on the given answer sheet. No additional (B) answer sheet will be issued.

Section–A

Long Answer Type Questions 2×19=38

***Note* :–** Section 'A' contains Five (05) Long-answer type questions of Nineteen (19) marks each. Learners are required to answer any *two* (02) questions only.

1. Design a Full Adder and clearly write the truth table for the Full Adder. Generate the Boolean expressions for Sum and Carry of the Full Adder. Also, draw a neat and labeled circuit diagram for the Full Adder.

2. Write short notes on the following :

   (a) Magnetic Hard Disk

   (b) Optical Disk

   (c) Memory Size

   (d) RAM

   (e) SRAM

   (f) DRAM

3. What are logic gates ? Describe basic gates with Truth Table and symbolic diagram.

4. Explain Boolean law and properties in detail and explain De Morgan's theorem with proof.

5. (i) Explain the Significance of K-map in Boolean Simplification. Explain 2-variable, 3-variable and 4-variable k-map.

   (ii) Minimize the following function in SOP minimal form using K-Maps :

   F (A, B, C, D) = $m(1, 2, 6, 7, 8, 13, 14, 15)$

   $d(0, 3, 5, 12)$

Section–B

Short Answer Type Questions 4×8=32

***Note* :–** Section 'B' contains Eight (08) Short-answer type questions of Eight (08) marks each. Learners are required to answer any *four* (04) questions only.

1. Give difference between combinational circuit and sequential circuits.

2. Convert each of the following binary numbers to decimal number.

   (I) $(111011101)_2$

   (II) $(10101010111)_2$

   (III) $(111100000)_2$

3. Define ROM and RAM ? Explain the different types of ROM and RAM.

4. Show the truth table for NAND gate along with symbolic diagram.

5. Obtained the simplified expression in (i) SOP (ii) POS form

$$F = x'z' + y'z' + yz' + xyz$$

6. Design the circuit for (P'Q) + (P + R') using basic gates.

7. What is Encoder ? Differentiate between decoder and encoder.

8. Obtained SOP form :

   (I) F = A'B'D' + A'CD + A'BC

   (II) d = A'BC'D + ACD + AB'D'

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