K–1002

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MCS–602/MIT(CS)–404

(MCA/MSCCS) IIIrd/IVth Semester Examination Dec., 2023

COMPUTER SYSTEM ARCHITECTURE/ COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 2 Hours] [**Max. Marks :** 70

Note* :–** This paper is of Seventy (70) marks divided into two (02) Sections 'A' and 'B'. Attempt the questions contained in these Sections according to the detailed instructions given there in. ***Candidates should limit their answers to the questions on the given answer sheet. No additional (B) answer sheet will be issued.

Section–A

Long Answer Type Questions 2×19=38

***Note* :–** Section 'A' contains Five (05) Long-answer type questions of Nineteen (19) marks each. Learners are required to answer any *two* (02) questions only.

1. (a) Explain computer system and computer architecture with suitable diagram.

   (b) Define subroutine and subroutine call. Explain with an example how stack used for handling subroutine call and return.

2. (a) Explain Micro-operation and their RTL specification in details with example.

   (b) Explain the Concepts of semiconductor memory and organization of memory modules.

3. (a) Explain the working of keyboard and video display unit. Also explain, what are the routine to control them ?

   (b) Explain DMA and DMA controller in detail.

4. Define Parallel processing concept with example. Write Parallelism algorithm for multiprocessor systems.

5. (a) Explain pipeline hazards and pipeline architecture.

   (b) What is deadlock ? Explain scheduling in multiprocessor systems.

Section–B

Short Answer Type Questions 4×8=32

***Note* :–** Section 'B' contains Eight (08) Short-answer type questions of Eight (08) marks each. Learners are required to answer any *four* (04) questions only.

1. Explain Machine level and Assembly level programming with example.
2. Explain Working of ALU with suitable example.
3. What is an instruction ? Explain interpretation and execution of an Instruction with example.
4. Explain Hardwired control and Microprogrammed control for CPU design.
5. Explain various addressing modes.
6. Explain the concept of memory management and Virtual memory in details.
7. Explain in details RISC with example of an existing RISC procession.
8. Explain Cache in multiprocessor systems and Cache coherence protocols.

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